

EE 435

Name _____

Exam 1

Spring 2020

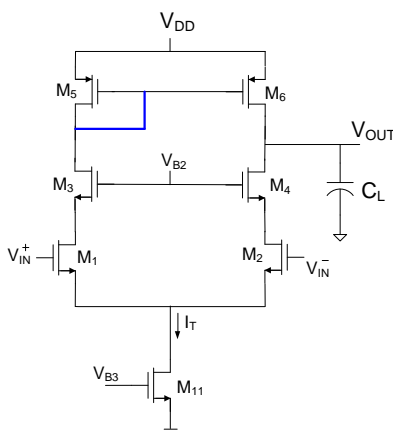
Due Friday March 27 at 5:00 p.m. – Upload as a .pdf file in Canvas

Instructions: The points allocated to each problem are as indicated. Note that the first and last problem are weighted more heavily than the rest of the problems. On those problems that need technology parameters that are not given in the problem, assume you are working in a $0.18\mu\text{m}$ CMOS process with process parameters $\mu_n C_{OX} = 350\mu\text{A}/\text{V}^2$, $\mu_p C_{OX} = 70\mu\text{A}/\text{V}^2$, $V_{Tn} = 0.5\text{V}$, $V_{Tp} = -0.5\text{V}$, $C_{OX} = 8\text{fF}/\mu^2$, $\lambda = 0.01\text{V}^{-1}$, $\gamma = 0$, and $A_{VT0} = 20\text{mV}\cdot\mu\text{m}$ for both n-channel and p-channel devices.

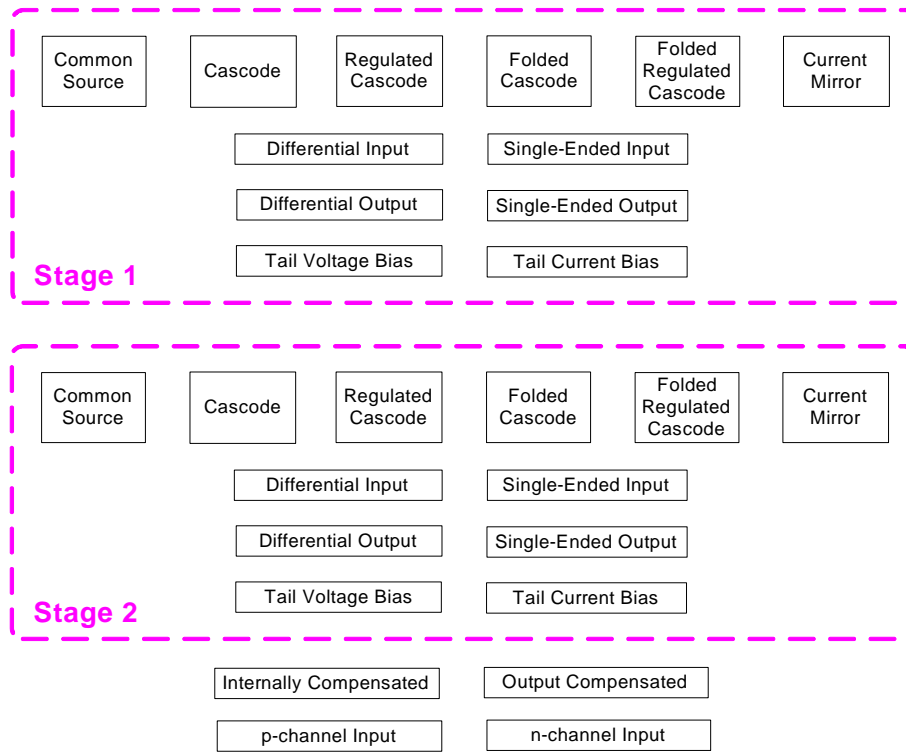
As a take-home exam, all work on this exam must be done individually. There should be no collaboration with anyone except for the course instructor, R. Geiger or the teaching assistants Bryce and Kwabena. If there are any questions, it might be easiest to address them by email to the course instructor. An immediate response can not be promised but I will check my email periodically throughout the duration of this exam.

Problem 1 (20 points) The operational amplifier has been designed with $|V_{EB}| = 150\text{mV}$ for all transistors with a total power dissipation of 20mW when biased with a single 5V supply (i.e. $V_{DD} = 5\text{V}$). The load capacitor is $C_L = 10\text{pF}$ and the length of all transistors are $2\mu\text{m}$.

- Determine the GB of the op amp
- What is the W/L ratio of M_1 ?
- Determine an acceptable value for V_{B2}
- Express the dc gain in terms of the small-signal model parameters of the devices.
- Give a numerical value for the dc gain of this op amp.
- What is the 3dB bandwidth?
- What is the slew rate of the op amp?



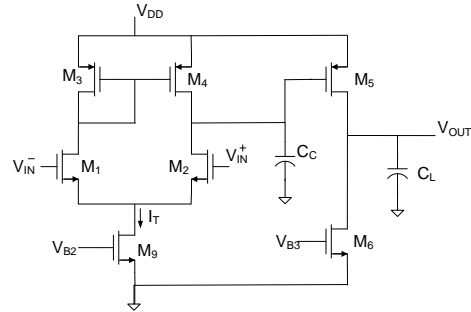
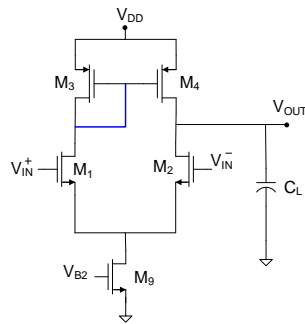
Problem 2 (10 points) A large number of different op amp architectures were identified in class. A table summarizing some of the more popular possible structures is shown below.



- Give the schematic of a two-stage op amp with a folded cascode first stage, a common source second stage, with differential inputs and single-ended output on the first stage. Use p-channel inputs on the first stage and n-channel inputs on the second stage. Use tail current bias on the first stage and tail voltage bias on the second stage. Use output compensation. Assume the total output capacitance (including any compensation capacitance) is C_L .
- Give an expression for the dc gain of the amplifier in part a) in terms of the small signal model parameters and in terms of the practical design parameters.
- Give an expression for the GB of the amplifier in terms of the small signal model parameters and in terms of the practical design parameters.

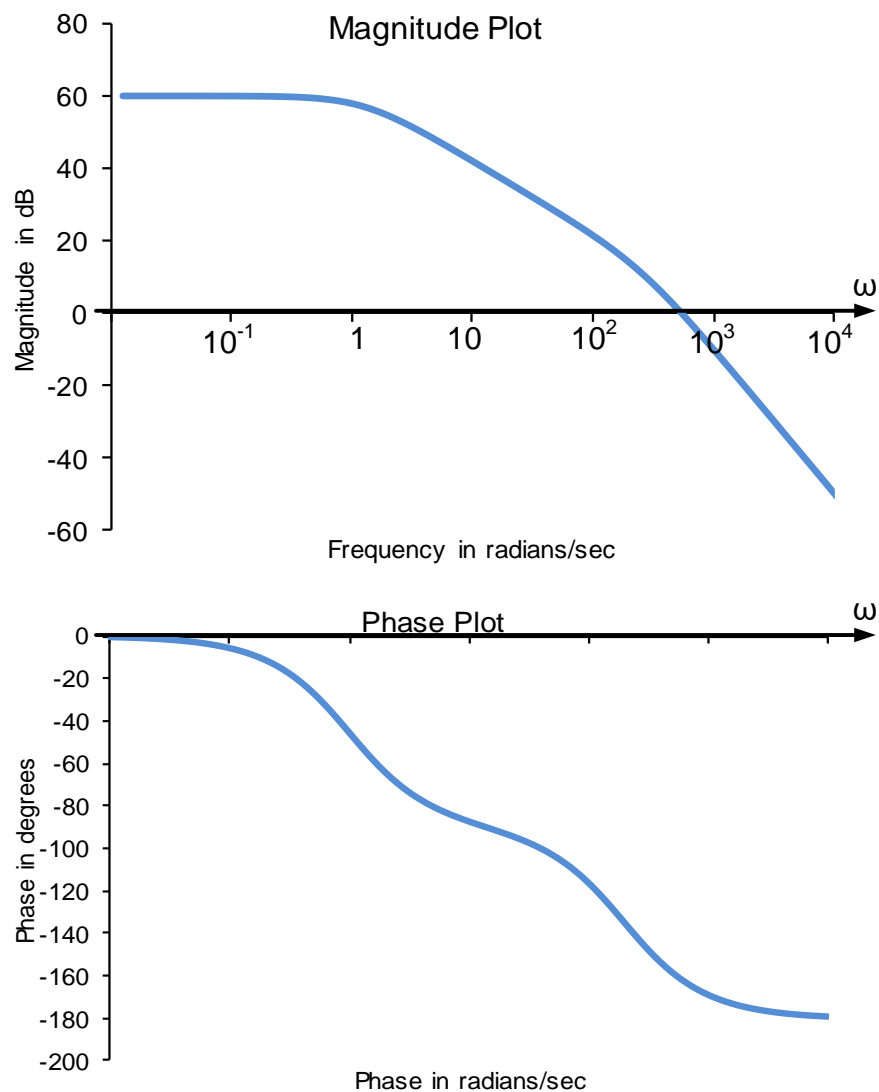
Problem 3 (10 points) Consider the two operational amplifiers shown below denoted as the 5T and the 7T op amps respectively. Assume the load capacitance is fixed and the 5T op amp is compensated with the dominant pole on the output node of the first stage with the compensation capacitor C_c with a pole spread of $3\beta A_0$ where A_0 is the dc voltage gain of the 7T op amp.

- Obtain an expression for the GB of the two amplifiers in terms of the small-signal model parameters
- Obtain an expression of the GB of the two amplifiers in terms of the practical parameters $\{V_{EB1}, V_{EB5}, P, \text{ and } \theta\}$ where P is the total power dissipation and for the 5T amplifier, θ is the fraction of the total power dissipated in the second stage.
- If both are connected in a unity-gain feedback configuration to serve as a buffer (i.e. $\beta=1$), compare the power efficiency of the two amplifiers. When making this comparison, pick θ to optimize the power efficiency of the 7T feedback amplifier.



Problem 4 (10 points) The magnitude and phase plots of a differential input, single-ended output all-pole operational amplifier are shown below.

- Determine the phase margin if this is used in a feedback amplifier with a feedback factor of $\beta=0.05$
- Is the feedback amplifier stable? Why?
- What is the maximum value of β that can be used if the amplifier is to have a 75° phase margin?
- If $\beta = 0.05$, what is the ideal dc closed loop gain if configured as a basic noninverting feedback amplifier and what is the percent closed-loop gain error due to the finite dc gain limitations of the op amp?
- How many poles does this amplifier have?



Problem 5 (10 points) Generate the Nyquist plot for the amplifier of Problem 4 if $\beta = 0.05$

Problem 6 (10 points) An all-pole amplifier has two open-loop poles, one at 10Hz and the other at 1MHz and the dc gain of the amplifier is 80dB. If used in a feedback application in a closed-loop amplifier with $\beta=0.5$, determine the

- phase margin
- Q of the closed loop poles

Assume the closed-loop gain satisfies the standard Black feedback expression

$$A_{FB} = \frac{A(s)}{1 + \beta A(s)}$$

where $A(s)$ is the open-loop gain of the op amp.

Problem 7 (10 points) Consider a feedback amplifier where the gain with feedback satisfies the standard Black feedback equation $A_{FB} = \frac{A(s)}{1 + \beta A(s)}$. Assume further that the open-loop amplifier is a two-pole amplifier with gain $A(s) = \frac{A_0}{\left(\frac{s}{\rho_1} + 1\right)\left(\frac{s}{k\rho_1} + 1\right)}$ where k

is the ratio of the open-loop poles.

- Sketch a root locus plot of the closed-loop poles for $0 < \beta < 1$. In this sketch, assume the pole ratio k satisfies the relationship $k \gg 1$.
- Determine the Q of the closed-loop poles if $\beta=0.5$, $A_0=10,000$ and $k=15,000$.

Problem 8 (20 points) A two-stage operational amplifier is shown. Assume $V_{DD}=2.5V$. Assume that the total power dissipation is 5mW.

- Size M_7 and determine V_{XX} so that V_{EB7} is 150mV.
- Size M_6 so that the power in the second stage is 10 times the power in the first stage.
- With the constraints given in the problem and in steps a)-b), identify the number of degrees of freedom remaining in the design of this circuit. With these constraints, complete the design leaving one degree of freedom to determine C_C .
- Determine C_C in your design so that the magnitude response is maximally flat if connected in a noninverting feedback configuration with $\beta=0.2$. Assume $C_L=500fF$ and assume the β network does not load the amplifier.
- Determine the GB of your design
- Determine the common-mode input range and the output range of your amplifier.

